Amendments to the Drawings

The attached drawing sheet includes changes to Fig. 3. This sheet, which includes Fig. 3, replaces the original sheet including Fig. 3. In Fig. 3, a typographical error has been corrected. No new matter has been added

Attachment: Replacement Sheet (1)

REMARKS

Applicants respectfully traverse and request reconsideration.

The drawings are objected to due to typographical errors. Applicants submit herewith a replacement sheet for FIG. 3 correcting the typographical error.

Claims 2, 6, 10 and 18 are objected to due to informalities. Applicants have corrected the informalities in these claims and in others.

Claims 1-4, 9-12 and 17-20 stand rejected under 35 U.S.C. §102(b) as being anticipated by Bowen et al. (U.S. Patent No. 6,292,200). As to claims 1, 9 and 17, Applicants have amended certain portions of the claims to include inherent language since the claims are directed to a graphics chip, such as an integrated circuit that at least performs graphics processing. The Bowen reference appears to have been misapprehended. For example, the Bowen reference is directed to a computer graphics system that has a hyper pipeline architecture that connects multiple host processor based rendering systems. Each rendering system can render primitives of an entire frame or a portion thereof. As described in Bowen, each "rendering pipe" is actually a separate host processor and application program based system. (See column 3, lines 3-6; column 6, lines 12-14 and 20-23; and column 7, lines 30-33). As such, the Bowen system appears to be a large and complex system that employs numerous host processors, corresponding applications and corresponding rasterizers, geometry engines, that are each coupled to another host based system through a unidirectional ring topology referred to as a hyper pipe network link.

In contrast, Applicants' claims are directed to an integrated circuit based system such as an integrated circuit that at least performs graphics processing that employs, among other things, backend circuitry that includes multiple parallel pipelines. In addition, a front end is used to

output the geometry to the backend that includes the multiple parallel pipelines. No such structure or operation is described in Bowen. For example, in the office action, the alleged front end is indicated to be host processor 301. This host processor, however is not in a graphics chip as required, for example, in claim 1 and instead is a separate host processor which is required for each "pipeline" so that multiple host processors are actually required. Moreover or alternatively, the host processor in Bowen does not provide rendering instructions to a backend that includes multiple pipes on a graphics chip. To the contrary, the host processor provides geometry information to only a single "pipeline". As noted above, the "rendering pipes" of Bowen are actually host processor based systems that are grouped together in a unidirectional network. Accordingly, Applicants respectfully submit that the claims are in condition for allowance.

With respect to claims 2, 10 and 18, again there is no graphics chip that includes multiple parallel pipelines described in the Bowen reference. As such, Applicants respectfully submit that the claims are in condition for allowance.

As to claims 3, 11 and 19, Applicants again respectfully submit that these claims are allowable at least as depending from an allowable base claim. In addition, the geometry described in claim 3 is provided by a front end that is coupled to a backend in a graphics chip. Again, no such structure of this type is described in the cited portions of the reference and as such, the claims are in condition for allowance.

With respect to claims 4, 12 and 20, again Applicants note that there is no graphics chip described in the cited portions that include a FIFO unit for load balancing each of the pipelines in the backend of a graphics chip. As such, these claims are also in condition for allowance.

Claims 5-8, 13-16 and 21-24 stand rejected under 35 U.S.C. §103(a) as being unpatentable over a single reference, namely Bowen et al. As to claims 5, 13 and 21, the claims

require that each of the parallel pipelines in the backend of the graphics chip, for example, includes a scan converter, a rasterizer, a unified shader and a texture unit. Again, no such graphics chip structure is described in the cited portions and as such, these claims are also in condition for allowance.

As to claims 6, 14 and 22, and claims 7, 8, 15, 16, 23 and 24, Applicants respectfully submit that these claims are also in condition for allowance for the relevant reasons given above.

Applicants respectfully submit that the claims are in condition for allowance and respectfully request that a timely Notice of Allowance be issued in this case. The Examiner is invited to contact the below-listed attorney if the Examiner believes that a telephone conference will advance the prosecution of this application.

Respectfully submitted,

Date: 7-10-07

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